Three new options are available to expand the capabilities of Keithley’s Model 4200-SCS, the industry’s leading interactive semiconductor characterization system. These options can be included with new systems or as factory upgrades to existing units.

**Dual-Channel Pulse Generator**

The Model 4200-PG2 Dual-Channel Pulse Generator integrates pulsing with the Model 4200-SCS’s DC source and measure capabilities. It provides voltage pulses as short as 20ns in high speed mode or up to ±20V (into 50Ω) in high voltage mode. Adding the 4200-PG2 to the Model 4200-SCS expands the system’s range of applications significantly, including:

- Charge pumping for interface charge trap characterization
- AC stress for stress/measure reliability testing
- Basic clock generation for test vectoring and failure analysis
- Digital triggering for multi-pin device testing

Using a supplied User Test Module (UTM), it’s simple to incorporate pulse generation into KITE test sequences. The pulse generator can also be driven as a stand-alone pulser for maximum flexibility and ease of use with the supplied Graphical User Interface (GUI). Support is provided for controlling a wide range of operating variables, including pulse frequency, duty cycle, rise/fall time, amplitude, and offset, as well as the ability to trigger single pulses and/or pulse trains.

**Digital Oscilloscope**

The Model 4200-SCP2 Oscilloscope offers both general purpose scope capabilities and time-domain measurements to complement the pulser’s time-domain sourcing. The scope can be programmed for automated measurement and data acquisition or used with the stand-alone GUI application provided to perform traditional oscilloscope tasks. The scope makes measurements in both the time (frequency, rise/fall time) and voltage domains (amplitude, peak-peak, etc.) The measurements can be applied to the entire captured waveform or a selected portion of the waveform by setting cursors.

**Pulse I-V Package**

The Pulse I-V package combines the PG2 dual-channel pulse generator, the SCP2 oscilloscope, the specialized interconnect, and patent-pending software to provide a turnkey Pulse I-V solution. The software controls sourcing from the pulse generator and data acquisition to automate a variety of pulse I-V tests. The Model 4200’s proven interface handles instrument setup and control, as well as data storage and presentation. The innovative software provides both cable compensation and load-line compensation, producing DC-like IV transistor curves, such as \( V_{DS} - I_D \) family of curves and \( V_{GS} - I_D \) for voltage threshold extraction. This solution provides pulse I-V testing for devices with self-heating issues, such as high power transistors and advanced CMOS on SOI technology. The Pulse I-V package includes sample projects to address the charge trapping problems for high \( \kappa \) gate structures. The specialized interconnect solves most of the problems encountered in high speed pulse testing, such as:

- Combining pulse and DC sources to a single DUT pin to permit both DC and pulse characterization without any re-cabling or switching
- Impedance matching to minimize reflection and maintain pulse fidelity
- Straightforward cabling and connection to DUT provides easy setup

The Pulse I-V package provides the user with an easy-to-understand solution right out of the box, while offering access to the pulse generator and scope for general purpose pulse and scope applications.
Pulse and Pulse I-V Options for the Model 4200-SCS

Technical Data Sheet Addendum

4200-PIV Specifications

<table>
<thead>
<tr>
<th>PULSE/LEVEL</th>
<th>HIGH SPEED</th>
<th>HIGH VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMPLITUDE</td>
<td>50 Ω into 50 Ω</td>
<td>100 mV p-p to 10 V p-p</td>
</tr>
<tr>
<td></td>
<td>50 Ω into 1 MΩ</td>
<td>200 mV p-p to 20 V p-p</td>
</tr>
<tr>
<td>DC LEVEL</td>
<td>±(3% + 50 mV)</td>
<td>±3% + 100 mV</td>
</tr>
<tr>
<td>RESOLUTION</td>
<td>1 mV</td>
<td>5 mV</td>
</tr>
<tr>
<td>OUTPUT CONNECTORS</td>
<td>SMA</td>
<td>SMA</td>
</tr>
<tr>
<td>SOURCE IMPEDANCE</td>
<td>50 Ω nominal</td>
<td>50 Ω nominal</td>
</tr>
<tr>
<td>SHORT CIRCUIT CURRENT</td>
<td>±200 mA</td>
<td>±800 mA peak</td>
</tr>
<tr>
<td>BASELINE NOISE</td>
<td>±(0.1 % + 5 mV) RMS</td>
<td>±(0.1 % + 5 mV) RMS</td>
</tr>
<tr>
<td>OVERSHEEI/PRE-SHOT/RINGING</td>
<td>±5% of amplitude ±20 mV</td>
<td>±5% of amplitude ±80 mV</td>
</tr>
<tr>
<td>OUTPUT LIMIT</td>
<td>Programmable limit to protect the DUT</td>
<td></td>
</tr>
</tbody>
</table>

TIMING

<table>
<thead>
<tr>
<th>FREQUENCY RANGE</th>
<th>HIGH SPEED</th>
<th>HIGH VOLTAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>TIMING RESOLUTION</td>
<td>1 Hz to 50 MHz</td>
<td>1 Hz to 2 MHz</td>
</tr>
<tr>
<td>RMS JITTER (period, width)</td>
<td>10 ns</td>
<td>10 ns</td>
</tr>
<tr>
<td>PERIOD RANGE</td>
<td>20 ns to 1 s (See Figure 1)</td>
<td>500 ns to 1 s</td>
</tr>
<tr>
<td>PULSE WIDTH RANGE</td>
<td>10 ns to (period – 10 ns)</td>
<td>250 ns to (period – 100 ns)</td>
</tr>
<tr>
<td>PROGRAMMABLE TRANSITION TIME</td>
<td>(0 – 100%)</td>
<td>100 ns – 1 s</td>
</tr>
<tr>
<td>TRANSITION SLEW RATE</td>
<td>Accuracy</td>
<td>±1% for transition time ≥100 ns</td>
</tr>
<tr>
<td></td>
<td>Linclarity</td>
<td>3% for transition time ≥100 ns</td>
</tr>
<tr>
<td>TYPICAL MIN. TRANSITION TIME (10–90%)</td>
<td>&lt; 15 ns</td>
<td>&lt; 150 ns</td>
</tr>
</tbody>
</table>

Figure 1. Permitted area of operation.

Pulse interface GUI for general purpose pulse operations.
4200-PIV
4200-PG2
4200-SCP2

4200-SCP2 Specifications

ANALOG INPUT
CHANNELS QUANTITY: 2.
BANDWIDTH (50Ω): DC to 1GHz.
BANDWIDTH (1MΩ): DC to 500MHz.
MAXIMUM INPUT (50Ω): ±5VDC, input load protection @ ±5VDC.
MAXIMUM INPUT (1MΩ): ±150 DC, derated 20dB/decade above 1MHz.
FULL SCALE INPUT RANGE (50Ω): 0.05, 0.1, 0.25, 0.5, 1, 2, 5, 10 (Vp-p).
FULL SCALE INPUT RANGE (1MΩ): 0.1, 0.2, 0.5, 1, 2, 5, 10, 20, 50, 100 (Vp-p).
DC GAIN ACCURACY: <±1% of full scale.
IMPEDANCE: 1MΩ || 12pF or 50Ω.
IMPEDANCE ACCURACY: ±1%.
COUPLING: DC or AC.
OFFSET ADJUST: ±(full scale range/2).
OFFSET ACCURACY: ±(1% offset + 1% full scale).
INPUT CONNECTOR: BNC.

ANALOG-TO-DIGITAL CONVERTER
RESOLUTION: 8-bit.
SAMPLE RATE: 2.5kS/s to 1.25GS/s in 1, 2.5, 5 steps. 2.5GS/s (1 channel interleaved).
ACQUISITION TIME RANGE: 50ns to 419 seconds.
ACQUISITION MODES: Normal, Average, Envelope, and Equivalent-Time.

TRIGGER
TRIGGER SOURCE: Channels 1 to 2, External, Pattern, Software.
POST-TRIGGER DELAY: 0 to 655 seconds.
PRE-TRIGGER DELAY: 0 to waveform time.
TRIGGER HOLD OFF RANGE: 0 to 655 seconds.
TRIGGER MODES: Edge or Pulse Width.
EDGE TRIGGER MODE: Rising or Falling Edge.
PULSE WIDTH RANGE: 20ns to 655 seconds. 10ns resolution.
EXTERNAL TRIGGER INPUT: TTL compatible, 10kΩ input impedance.
CONNECTOR: SMB.

OPTIONAL SCOPE PROBE: 4200-SCP2-ACC
BANDWIDTH: 500MHz.
MAX. DC: 600V DC rated.
LENGTH: 1 meter.
ATTENUATION: 10Ω fixed.
LOADING: 8pF and 10MΩ.
CONNECTOR: BNC.

Scope interface GUI for general purpose scope operations.

Optional scope probe (4200-SCP2-ACC).
### 4200-PIV Typical Specifications

#### CHANNLES: 2

**TYPICAL PULSE PERFORMANCE:**

<table>
<thead>
<tr>
<th>Measurement</th>
<th>With 4200 Remote Bias Tee</th>
<th>Without 4200 Remote Bias Tee (Figure 3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Accuracy</td>
<td>&lt;1% of signal ±1mV</td>
<td>N/A</td>
</tr>
<tr>
<td>Max. Current (PW = 40–150 ns)</td>
<td>100 mA @ PW = 40 ns</td>
<td>100 mA @ PW = 40 ns</td>
</tr>
<tr>
<td>Resolution</td>
<td>Maximum 5µA, 250µV</td>
<td>Maximum 5µA, 250µV</td>
</tr>
<tr>
<td></td>
<td>8-bit A/D converter</td>
<td>8-bit A/D converter</td>
</tr>
<tr>
<td>Sample Rate</td>
<td>1.25 Gsample/s</td>
<td>1.25 Gsample/s</td>
</tr>
<tr>
<td>Duty Cycle</td>
<td>&lt;0.1%</td>
<td>&lt;0.1%</td>
</tr>
<tr>
<td>DC Offset</td>
<td>±200 mV</td>
<td>N/A</td>
</tr>
<tr>
<td>Min. Transition Time</td>
<td>10 ns²</td>
<td>See PG2 specs</td>
</tr>
<tr>
<td>Maximum V</td>
<td>10 Vpp into 50Ω²</td>
<td>10Vpp into gate, 40Vp into drain</td>
</tr>
<tr>
<td>Max. Pulse Width</td>
<td>150 ns</td>
<td>See PG2 specs</td>
</tr>
</tbody>
</table>

**SMU TYPICAL DC PERFORMANCE (with 4200 Remote Bias Tee):**

- Leakage: 1–10mA/V
- Noise: 1–10mA RMS
- Max. Voltage: 200V (>40V requires safety interlock and related precautions)
- Max. Current: 0.5A

**4200 REMOTE BIAS TEE TYPICAL PERFORMANCE:**

- Band Pass: 10kHz–300MHz (3dB)
- Power Divider Max. Power Input: 0.125W DC

#### NOTES

1. Unless stated otherwise, all specifications assume a 50Ω termination.
2. Level specs are valid after 50ns typical settling time (after slewing) for the high speed mode and after 500ns typical settling time (after slewing) for the high voltage mode into a 50Ω load.
3. Specs apply to a 10–90% transition, typical.
4. Inputs are referenced to 4200 chassis ground.
5. Leakage measured after a five-second settling time.
6. All typical specs apply to the AC+DC output connector of the 4200 Remote Bias Tee interconnect box and after system compensation.
7. 4200 Remote Bias Tee supports the 4200-PG2 high speed range only.

All specifications apply at 23° ±5°C, within 1 year of calibration, RH between 5% and 60%, after 30 minutes of warmup.

Specifications are subject to change without notice. Refer to www.keithley.com for the latest product information.

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**Figure 2. Interconnect for pulse I-V (high < charge trapping and isothermal testing).**

**Figure 3. Interconnect for single pulse charge trapping.**