Gate insulation and surface pasivation of III-N and III-V-based transistors.

One of the major factors that limits the performance and reliability of III-N high electron mobility transistors (HEMTs) for high power radio-frequency (RF) and high temperature applications is the high gate leakage due to the surface defects and a finite barrier height. To solve this problem, significant progress has been made on metal-oxide-semiconductor high electron mobility transistors (MOS HEMTs) using SiO_2, Si_3N_4, Al_2O_3 and other oxides. Al_2O_3 is an attractive material for use in the gate dielectric layer of MOS HEMTs. We investigated Al_2O_3 layers prepared by a low temperature atomic layer deposition (ALD). This technique allows us to use a photoresist to fabricate a self-aligned metal/oxide stack. Moreover, there is a possibility to use different oxide layers or processing steps in the gate stack and for the passivation of the access region of the transistors, see Fig.1.

Other attractive III-V material systems for MOS HEMTs are heterostructures based on GaAs or InP. Technology for preparation of gate-insulating oxide layer and engineering of the oxide/semiconductor interface represents one of the major challenges as it is in tight relation with density of trap states. To address this issue, various promising approaches were studied, e.g. deposition of interface-passivation layers (AlP, InP, AlO_x, Ga_2O_3/Gd_2O_3) or oxide layers (Al_2O_3) prepared by atomic layer deposition (ALD). Scope of our research includes GaAs/InGaAs heterostructure metal-oxide-semiconductor field-effect transistors (MOSHFET) with emphasis on oxide/GaAs layers optimisation. Recently, we studied effects of low-invasive GaAs oxidation techniques, i.e. O_2 plasma-assisted oxidation and UV-assisted wet oxidation (photowashing), and passivation of GaAs surface with AlO_x layer prepared in-situ from MOCVD-grown, air-oxidised Al layer, see Fig.2. These layers are intended to form high-quality oxide/GaAs interface that can serve either as a passivation or gate dielectric after being covered with suitable high-κ material.

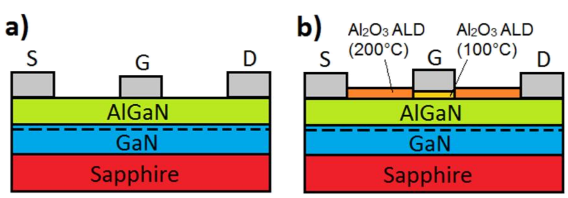

Fig. 1 Self-aligned AlGaN/GaN MOS HEMT.

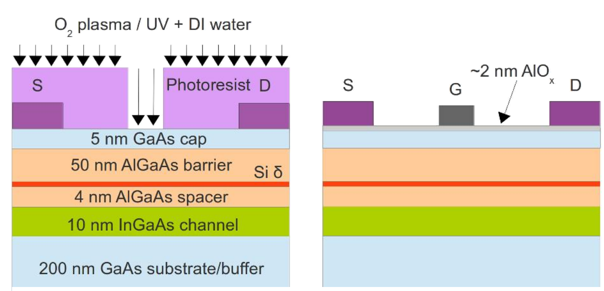

Fig.2 Oxidation of gate trenches in III-V HEMTs

Further reading:

Blaho, M., et al : Self-aligned normally-off metal-oxide-semiconductor n++GaN/InAlN/GaN high-electron mobility transistors. Phys. Status Solidi A 112 (2015) 1086-1090.

Blaho, M., et al : Ni/Au-Al2O3 gate stack prepared by low-temperature ALD and lift-off for MOSHEMTs. Microelectr. Engn. 112 (2013) 204-207.

Gucmann, F., et al: III-As heterostructure field-effect transistors with recessed ex-situ gate oxide by O_2 plasma-oxidized GaAs cap. J. Vacuum Sci Technol. B 33 (2015) 01A111.

Gucmann, F., et al : InGaAs/GaAs metal-oxide-semiconductor heterostructure field-effect transistors with oxygen-plasma oxide and Al_2O_3 double-layer insulator. Applied Phys. Lett. 105 (2014) 183504.