Monday, June 28

8.30 Welcome

8.40 Plenary talk

Invited Talk: ***Oxides beyond SiO_2 for Microelectronics***

D. Schlom

Department of Materials Science and Engineering, Cornell University, Ithaca, New York

1.4 Emerging dielectric materials

Chair: T. Schröder

9.10 **Invited Talk:** ***Giant electroresistance and electrical control of spin-polarization with ferroelectric tunnel barriers***

M. Bibes[1], V. Garcia[1,2], S. Fusil[1], K. Bouzehouane[1], C. Deranlot[1], L. Bocher[3], Sh. Enouz-Vedrenne[3], A. Gloter[3], D. Imhoff[3], N. Mathur[2], A. Barthélémy[1]

1 - Unité Mixte de Physique CNRS/Thales, Université Paris-Sud, Orsay, France.
2 - Department of Materials Science, University of Cambridge, UK
3 - Laboratoire de Physiques des Solides, Université Paris Sud, CNRS UMR Orsay, France
4 - Thales Research &Technology, Palaiseau, France

9.40 **Invited Talk:** ***Electrical properties and nanodomain structure of ferroelectric/paraelectric superlattices***

P. Zubko, N. Stucki, C. Lichtensteiger, J.-M. Triscone

DPMC, University of Geneva 24, Switzerland

10.10 ***Spectroscopic detection of spin-polarized bands and hopping-induced mixed valency in metallic $GdSc_{1-x}Ti_xO_3$ peroskite alloys with x = 0.18 and 0.25: spin alignment differences in nano-grain and single crystal epitaxial thin films***

G. Lucovsky[1], L. Miotti[1], K. Paz Bastos[1], C. Adamo[2], D. G. Schlom[2,3]

1 - North Carolina State University, Raleigh, NC, USA
2 - Penn State University, State College, PA, USA
3 - Cornell University, Ithaca, NY, USA

10.30 ***Determination of the energy band structure of TiN/GdSiO/Si MOS capacitors***

H.D.B Gottlob[1], H.M. Przewłocki[2], and H. Kurz[1]

[1]- Advanced Microelectronic Center Aachen (AMICA), AMO GmbH, Aachen, Germany
[2]- Institute of Electron Technology, Warsaw, Poland

10.50 - 11.20 Break

Monday, June 28

1.2 Advanced technologies for thin dielectric film growth

Chair: C. Kügeler

11.20 **Invited Talk**: ***Atomic layer deposition of high-k oxides – an overview of current state and challenges***

M. Ritala, J. Niinistö, K. Kukli and M. Leskelä

Department of Chemistry, University of Helsinki, Finland

11.50 ***Atomic layer deposition of HfO_2 and Al_2O_3 films on 300 mm Si wafers for gate stack technology***

R. Lupták[1], J.M.J. Lopes[1], St. Lenk[1], B. Holländer[1], E. Durğun Özben[1], A.T. Tiedemann[1], M. Schnee[1], U. Breuer[2], A. Besmehn[2], P.K. Baumann[3], M. Heuken[3], J. Schubert[1]and S. Mantl[1]

1 - Institute for Bio- and Nanosystems (IBN1-IT) and JARAFIT, Research Center Jülich, Germany
2 - Central Division of Analytical Chemistry (ZCH), Research Center Jülich, Germany
3 - AIXTRON AG, Herzogenrath, Germany

12.10 ***Effect of RE^{3+} cation size on properties of rare earth scandate films deposited by ALD***

M. Putkonen[1,2], P. Myllymäki[2], L. Niinistö[2], M. Roeckerath[3], J.M. Lopes[3], J. Schubert[3], K. Mizohata[4]

1 - Beneq Oy, Vantaa, Finland.
2 - Laboratory of Inorganic Chemistry, Aalto University School of Science and Technology Aalto, Espoo, Finland.
3 -Institute of Bio and Nanosystems, JARA-Fundamentals of Future Information Technologies, Research Centre Jülich, Germany.
4-Division of Materials Physics, Department of Physics, University of Helsinki, Finland

12.30 - 14.00 **Lunch**

Monday, June 28

2.1 High-k dielectrics on Si

Chair: A.C. Kummel

14.00 **Invited Talk:** ***Plenty of room at the bottom: scaling the high-k/silicon interfacial layer***

M. M. Frank[1], T. Ando[1], K. Choi[2], Ch. Choi[1,], J. Bruley[1], Ch. Marchiori[3], J. Fompeyrine[3], V. Narayanan[1]

1 - IBM T.J. Watson Research Center, Yorktown Heights, NY, USA
2 - GLOBALFOUNDRIES Inc., Yorktown Heights, NY, USA
3 - IBM Research GmbH, Zürich Research Laboratory, Rüschlikon, Switzerland

14.30 ***Microstructure, bonding states and band alignment of the $(Tb_xSc_{1-x})_2O_3$/Si system***

I. Geppert[1], M. Eizenberg[1], N. A. Bojarczuk[2], and S. Guha[2]

1 - Dpt. of Materials Engineering, Technion - Israel Institute of Technology, Haifa, Israel
2 - IBM Research Division, Yorktown Heights, New York

14.50 ***The onset of electrical stress in 3nm and 6nm molecular beam deposited $LaLuO_3$ MOSCAPs on n-Si(100) substrates using a TiN metal gate and Al back contact***

Y. Lai[1], S. Monaghan[1], K. Cherkaoui[1], H. D. B. Gottlob[2], M. Schmidt[2], J. Schubert[3], J. M. J. Lopes[3], and P. K. Hurley[1]

1 - Tyndall National Institute, University College Cork, Lee Maltings, Cork, Ireland
2 - AMO GmbH, AMICA, Aachen, Germany
3 - Institute of Bio and Nanosystems, JARA, Research Centre Juelich, Juelich, Germany

2.3 High-k/metal gate stack, characterisation, scaling, stability

15.10 ***Rare-earth based oxides/TiN gate stacks on high mobility strained SOI for fully depleted (FD) MOSFETs***

E. Durğun Özben[1], J. M. J. Lopes[1], A. Nichau[1], R. Lupták[1], S. Lenk[1], A. Besmehn[2], K. K. Bourdelle[3], Q.-T. Zhao[1], J. Schubert[1] and S. Mantl[1]

[1]*Institute for Bio- and Nanosystems (IBN1-IT) and JARA-FIT, Research Center Jülich, Germany*
[2]*Central Division of Analytical Chemistry (ZCH), Research Center Jülich, Germany*
[3]*SOITEC S.A., Parc Technologique des Fontaines, Bernin, France*

15.30 ***Trapping in GdSiO high-k films***

R. Rao[1], R. Simoncini[1], H. D. B. Gottlob[2], M. Schmidt[2], F. Irrera[1]

1 – Sapienza Università di Roma, Electronics Department and IU.NET
2 – Advanced Microelectronic Center Aachen, AMO GmbH, Aachen, Germany

15.50 ***Electrical characterization of high-k based MIS structures with negative resistance effect in I-V characteristics***

A. Gómez[1], H. Castán[1], H. García[1], S. Dueñas[1], L. Bailón[1], F. Campabadal[2], J. M. Rafí[2] and M. Zabala[2]

1 - Department of Electronics, University of Valladolid, E.T.S.I. Telecomunicación,
2 - Centro Nacional de Microelectrónica. Instituto de Microelectrónica Barcelona, Spain

16.10 - 16.40 **Break**

Monday, June 28

2.4 Defect characterisation, engineering of dielectrics, leakage currents

Chair: T. Hashizume

16.40 **Invited Talk:** ***Traps and trapping phenomena and their implications on electrical behavior of high-k capacitor stacks***

A. Paskaleva[1], M. Lemberger[2], E. Atanassova[1], A. J. Bauer[2]

1 - Institute of Solid State Physics, Bulgarian Academy of Sciences, Sofia, Bulgaria
2 - Fraunhofer Institute for Integrated Systems and Device Technology, Erlangen, Germany

17.10 ***Temperature dependence of the emission and capture times of SiON individual traps after positive bias temperature stress***

M. Toledano-Luque[1], B. Kaczer[1], Ph. Roussel[1], T. Grasser[3], and G. Groeseneken[1]

1 - Imec, Leuven, Belgium, 2 - UCM, Madrid, Spain, 3 - TU Wien, Austria

17.30 ***Capture cross sections for holes at LaLuO/Si interfaces***

O. Engström[1]**,** F. Ducroquet[2], B. Raeissi[1], J. Schubert[3], J. M. J Lopes[3], H. D. B. Gottlob[4]

1 – Department of Microtechnology and Nanosci, Chalmers Univ Technology, Göteborg
2 – Minatec, IMEP-LAHC, Grenoble
3 - Institute of Bio and Nanosystems, JARA, Research Centre Juelich,
4 – Advanced Microelectronic Center Aachen, AMO GmbH, Aachen

17.50 ***Defects in low-κ dielectrics and etch stop layers for use as interlayer dielectrics in ULSI***

B.C. Bittel[1], P.M. Lenahan[1], S. King[2]

1 – The Pennsylvania State University, 2 – Intel Corporation

18.10 ***Analysis of the effect germanium preamorphisation on interface defects and leakage current for high-k MOSFET***

G. Roll[1], S. Jakschik[1], M. Goldbach[2], A. Wachowiak[1], T. Mikolajick[1,3], L. Frey[4]

1 – Namlab gGmbH, Dresden, Germany
2 – Qimonda Dresden GmbH&Co. OHG , Dresden, Germany
3 – University of Dresden, Germany
4 – Fraunhofer IISB, Erlangen, Germany

1.5 New device approaches

18.30 ***Modelling of tunneling through a three-layer gate stack with/without a quantum well***

A. Mazurak, J. Walczak, and B. Majkusiak

Institute of Microelectronics and Optoelectronics, Warsaw Univ. Technology, Poland

18.50 ***Properties of SiO_2 and Si_3N_4 as gate dielectrics for printed ZnO transistors***

S. Walther[1], S. Polster[1], B. Meyer[1], M.P.M. Jank[2], H. Ryssel[1,2], L. Frey[1,2]

1 Chair of Electron Devices, University of Erlangen-Nuremberg, Erlangen, Germany
2 Fraunhofer Institute for Integrated Systems and Device Technology, Erlangen, Germany

19.10 **Poster session**

20.00 **Dinner**

Tuesday, June 29

2.2 High-k dielectrics on high mobility semiconductors: Ge

Chair: G. Lucovsky

8.00 **Invited Talk:** ***Dielectrics on high mobility substrates for aggressively scaled CMOS***

A. Dimoulas, D. Tsoutsou, G. Mavrou, Y. Panayiotatos, S. F. Galata , E. Golias, A. Sotiropoulos

MBE laboratory, Institute of Materials Science, NCSR DEMOKRITOS, Athens, Greece

8.30 ***Ge SB-p-MOSFETs with ALD ZrO_2/La_2O_3 dielectrics***

C. Henkel, S. Abermann, O. Bethge, G. Pozzovivo, and E. Bertagnolli

Institute for Solid State Electronics, Vienna, 1040 Austria

8.50 ***Epitaxial growth of Dy_2O_3 films on Ge(100) and $SrTiO_3$(100) substrates by molecular beam epitaxy***

Md. N. K. Bhuiyan[1], M. Menghini[1], J. W. Seo[2], J.-P. Locquet[1], Ch. Marchiori[3]

1 – Department of Physics and Astronomy, Katholieke Universiteit Leuven, Belgium
2 - Department of Metallurgy and Materials Engineering, Katholieke Universiteit Leuven
3 – IBM Research GmbH, Zurich Research Laboratory, Rueschlikon, Switzerland

2.2 High-k dielectrics on high mobility semiconductors: III-N

9.10 **Invited Talk:** ***Interface control technologies of GaN-based MOS structures for high-efficiency power switching transistors***

T. Hashizume, Y. Hori and C. Mizue

Research Center for Integrated Quantum Electronics (RCIQE), Hokkaido University, Japan
JST-CREST

9.40 ***Design rules of gate dielectric for GaN-based MIS−devices and performance of Al_2O_3/AlGaN/GaN and Al_2O_3/InAlN/GaN MOSHFETs***

P. Kordoš[1,2], R. Stoklas[1], M. Mikulics[3], D. Gregušová[1], A. Fox[3], K. Čičo[1], J. Novák[1], and K. Fröhlich[1]

1 – Institute of Electrical Engineering, Slovak Academy of Sciences, Bratislava, Slovakia
2 – Department of Microelectronics, University of Technology, Bratislava, Slovakia
3 – Institute of Bio- and Nanosystems (IBN-1), Research Centre Jülich, Germany

10.00 ***C-V characterization of ALD-Al_2O_3 insulated gates on AlGaN/GaN structure***

Ch. Mizue[1] and T. Hashizume[1,2]

1 –Research Center for Integrated Quantum Electronics (RCIQE), Hokkaido University, Sapporo, Japan
2 – JST-CREST

10.20 - 10.50 **Break**

Tuesday, June 29

2.2 High-k dielectrics on high mobility semiconductors: III-V

Chair: M.M. Frank

10.50 **Invited Talk:** ***Correlations between atomic and electronic structure of monolayer nucleation and unpinning of a compound semiconductor surface during atomic layer deposition***

J. B. Clemens[1], E. A. Chagarov[1], M. Holland[2], R. Droopad[3], J. Shen[1] and **A. C. Kummel**[1]

1 Dept. of Chem. and Biochem., Univ. of California, San Diego, La Jolla, California
2 Dept of Electronics & Electrical Engineering, University of Glasgow, Scotland, U.K.
3 Dept of Physics, Texas State University-San Marcos, Texas, U.S.A.

11.20 ***Improved Capacitance-voltage characteristics of MOS capacitors on unpassivated GaAs incorporating a PECVD deposited Si_3N_4 dielectric layer***

E. O'Connor, S. Monaghan, V. Djara, P. K. Hurley, and K. Cherkaoui

Tyndall National Institute, University College Cork, Ireland

11.40 ***Effect of processing of W gate on the quality of MOS capacitors on GaAs***

D. J.Webb, C. Marchiori, D. Caimi, C. Rossel, M. Richter, M. Sousa, C. Gerl, C. Andersson, and J. Fompeyrine

IBM Research-Zurich, 8803 Rüschlikon, Switzerland

12.00 ***Electrical characterisation of Pd/HfO_2 MOSCAPs with/without a thin Al_2O_3 or MgO interface control layer deposited on GaAs or $In_{0.53}Ga_{0.47}As$/InP by ALD***

A. O'Mahony[1], S. Monaghan[1], R. Chiodo[1,2], I. M. Povey[1], A. Blake[1], K. Cherkaoui[1], É. O'Connor[1], R. E. Nagle[1], R. D. Long[1], V. Djara[1], D. O'Connell[1], S. B. Newcomb[3], F. Crupi[2], P. K. Hurley[1] and M. E. Pemble[1]

1 - Tyndall National Institute, University College Cork, Ireland
2 - Università della Calabria, Arcavacata di Rende (CS), Italy
3 - Glebe Scientific Ltd., Glebe Laboratories, Newport, Ireland

12.20 ***Modeling the CV response of high-k/III-V systems: GaAs, $In_{0.53}Ga_{0.47}As$ and InAs***

T. O'Regan and P. K. Hurley

1 – Tyndall National Institute, University College Cork, Ireland

13.00 - 14.30 **Lunch**

14.30 - 19.00 **Social event - trip**

Wednesday, June 30

1.1 Theory of dielectric materials

Chair: M. Ritala

8.00 **Invited Talk:** ***Charge transfer multiplet theory and Tanabe-Sugano multiplet energy level diagrams applied to: (i) band edge electronic states, and (ii) O-atom vacancy defects in transition metal oxide gate dielectrics***

G. Lucovsky, L. Miotti, and K. Paz Bastos

North Carolina State University, Raleigh, USA

8.30 ***Multi-phonon hole-trapping from first-principles***

F. Schanovsky, W. Gös, and T. Grasser

CDL for TCAD, Institute for Microelectronics, TU Wien, Austria

2.5 Electrical characterisation and reliability of devices with alternative dielectrics

8.50 **Invited Talk:** ***Recent trends in bias temperature instability***

B. Kaczer[1], T. Grasser[2], J. Franco[1,3], M. Toledano-Luque[1,4], Ph. J. Roussel[1], G. Groeseneken[1,3]

1 – IMEC, 2 – TU Wien, 3 – KU Leuven, 4 – UC Madrid,

9.20 ***Dielectric BD in polycrystalline HfO_2 gate dielectrics investigated by CAFM***

V. Iglesias[1], M. Porti[1], M. Nafría[1], X. Aymerich[1], , P. Dudek[2], G. Bersuker[3]

1 - Dept. Eng. Elect.,Edifici Q, Universitat Autònoma de Barcelona, Spain
2- Innovations for High Performance Microelectronics (IHP), Frankfurt (Oder), Germany
3 - Sematech, USA

9.40 ***CV measurements on $LaLuO_3$ stack MOS capacitor using a new 3-pulse technique***

N. Sedghi[1], W. Davey[1], I. Mitrovic[1], J. M. J. Lopes[2], J. Schubert[2], and S. Hall[1]

1 – University of Liverpool, Liverpool, UK
2 - Institute of Bio and Nanosystems, Research Centre Juelich, Germany

10.00 - 10.30 **Break**

Wednesday, June 30

2.5 Electrical characterisation and reliability of devices with alternative dielectrics

Chair: A. Dimoulas

10.30 ***Deep-level transient spectroscopy on high-k dielectric stacks: Effects of the interlayer traps***

H. Castán, S. Dueñas, H. García, A. Gómez, and L. Bailón

Departamento de Electricidad y Electrónica, E.T.S.I.Telecomunicación, Universidad de Valladolid, Spain

10.50 ***Dielectric layers suitable for high voltage integrated trench capacitors***

J. vom Dorp[1], T. Erlbacher[2], A.J. Bauer[2], H. Ryssel[1,2], L. Frey[1,2]

1 – Chair of Electron Devices, University Erlangen-Nuremberg, Erlangen, Germany
2 - Fraunhofer Institute for Integrated Systems and Device Technology, Erlangen

11.10 ***Non-contact metrology for inversion charge carrier mobility by corona charge and photovoltage measurements on blank wafers with a gate dielectric***

J.L. Everaert[1], E. Rosseel[1], A. Pap[2], A. Meszaros[2], J. Dekoster[1], T. Pavelka[2]

1 IMEC, Leuven, Belgium
2 Semilab Semiconductor Physics Laboratory, Co., Ltd., Budapest, Hungary

11.30 ***Current Instabilities in REO-HfO_2 gate stacks grown on Germanium based MOS devices due to Maxwell-Wagner instabilities and dielectrics relaxation***

M. S. Rahman[1,2], E. K. Evangelou[2], A. Dimoulas[3], G. Mavrou[3] and S. Galata[3]

1 - GSI - Helmholtzzentrum für Schwerionenforschung, Darmstadt, Germany
2 - Lab of Electronics-Telecoms & Applications, Dept. of Physics, University of Ioannina, Greece
3 –MBE Laboratory, Institute of Material Science, NCSR«Demokritos», Greece

11.50 ***Processing dependences of CHC degradation on strained-Si pMOSFETs***

E. Amat[1], J.Martin-Martinez[1], M.B.Gonzalez[2], R.Rodriguez[1], M.Nafria[1], E.Simoen[2], P.Verheyen[2] and X.Aymerich[1]

1 – Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, Spain
2 – IMEC, Leuven Belgium

12.10 ***Gate oxide reliability at the nano-scale evaluated by combining cAFM and CVS***

T. Erlbacher[1], V. Yanev[1], M. Rommel[1], A.J. Bauer[1], L. Frey[1,2]

1 – Fraunhofer Institute for Integrated Systems and Device Technology, Erlangen, Germany
2 – Chair of Electron Devices, University of Erlangen-Nuremberg, Erlangen, Germany

12.30 - 14.00 Lunch

Wednesday, June 30

3.1 High-k dielectrics for MIM (DRAM etc.)

Chair: A. Paskaleva

14.00 **Invited Talk**: ***Metal-insulator-metal capacitors – intrinsic constrains of high-k dielectrics***

Ch. Wenger, M. Lukosius, G. Lupina, T. Schroeder

IHP, Im Technologiepark 25, 15236 Frankfurt/Oder, Germany

14.30 ***Electrical characteristics of TiTaO based MIM capacitors***

M. Lukosius[1], Ch. Wenger[1], G. Ruhl[2], S. Rushworth[3]

1 – IHP, Im Technologiepark, Frankfurt Oder, Germany
2 – Infineon, Regensburg, Germany
3 – SAFC HiTech, Bromborough, Wirral, Merseyside, U.K

14.50 ***Macroscopic and microscopic electrical characterization of high-k ZrO_2, $(ZrO_2)_x(Al_2O_3)_{1-x}$ and $ZrO_2/Al_2O_3/ZrO_2$ metal-insulator-metal structures***

D. Martin[1], M. Grube[1], W. Weinreich[2], J. Müller[2], L. Wilde[2], E. Erben[1], W.M. Weber[1], U. Schröder[1], Th. Mikolajick[1,3], and H. Riechert[4]

1 – Namlab gGmbH, Dresden, Germany
2 – Fraunhofer CNT, Dresden, Germany
3 – Chair of Nanoelectronic Materials, University of Technology Dresden, Germany
4 – Paul-Drude-Institut für Festkörperelektronik, Berlin, Germany

15.10 ***Atomic scale engineering of future high–k DRAM dielectrics: the example of partial Hf substitution by Ti in $BaHfO_3$***

P. Dudek[1], G. Lupina[1], P. Zaumseil[1], D. Schmeisser[2] and T. Schroeder[1]

1 – IHP, Frankfurt (Oder), Im Technologiepark 25, Germany
2 – BTU Cottbus, Germany

15.30 - 16.00 **Break**

Wednesday, June 30

3.2 Resistive switching in dielectrics

Chair: Ch. Wenger

16.00 **Invited Talk**: ***Nano structured resistive memory cells based on TiO_2 thin films***

C. Kügeler [a,b], S. Hoffmann-Eifert [a,b] and R. Waser [a,b]

[a] *Institut für Festkörperforschung, Forschungszentrum Jülich GmbH, Germany*
[b] *JARA- Fundamentals of Future Information Technology, Jülich, Germany*

16.30 ***CMOS compatible TiN/HfO_2/Ti/TiN MIM devices for future RRAM applications***

Ch. Walczyk,[1] T. Schroeder,[1] M. Lukosius,[1] D. Walczyk,[1] M. Fraschke,[1] A. Fox,[1] D. Wolansky,[1] B. Tillack,[1, 2] and Ch. Wenger [1]

[1]*IHP, Frankfurt (Oder), Germany*
[2]*Department of Computer Engineering and Microelectronics, TU Berlin, Germany*

16.50 ***Growth behaviour and characterization of atomic layer deposited TiO_x thin films for resistive switching memory cells***

M. Reiners, S. Hoffmann-Eifert, C. Kügeler, R. Bruchhaus and R. Waser

Institute for Solid State Research, Research Center Jülich GmbH and JARA-FIT, Jülich

3.3 Dielectrics for non-volatile memories (flash, nanocrystal-based memories,…)

17.10 ***Charge retention in CT SiN: impact of technology and operating conditions***

G.Ghidini[a], N.Galbiati[a], E.Mascellino[b], C.Scozzari[a], A.Sebastiani[a], S.Amoroso[b], C.Monzio, Compagnoni[b], A.S.Spinelli[b], A.Maconi[b], R.Piagge[a], A.Del Vitto[a], M.Alessandri[a], I.Baldi[a], E.Moltrasio[a], G.Albini[a], A.Grossi[a], P.Tessariol[a], E.Camerlenghi[a] and A.Mauri[a]

a Numonyx, Central R&D, Agrate Brianza, Italy
b Dipartimento di Elettronica e Informazione, Politecnico di Milano–IU.NET, Italy

17.30 ***Study of parasitic trapping in alumina used as blocking oxide for non volatile memories***

J. P. Colonna, M. Bocquet, G. Molas, N. Rochat, P. Blaise, H. Grampeix, C. Licitra, F. Martin, D. Lafond, L. Masoero, V. Vidal, J. P. Barnes, M Veillerot and K. Yckache

1 – CEA-LETI, Minatec, 17, Grenoble Cedex 9, France

17.50 ***Synthesis and characterization of $DyScO_x$ films deposited on Si and Si-rich SiN by atomic layer deposition for blocking layer replacement in TANOS stack***

A. Lamperti[1], E. Cianci[1], U. Russo[1,*], G. Congedo[1], O. Salicio[1], S. Spiga[1], M. Fanciulli[1,2]

1 – Laboratorio MDM, IMM-CNR, Agrate Brianza (MB) Italy
2 – Dipartimento di Scienza dei Materiali, Università degli Studi di Milano Bicocca, - Italy
** Now with Numonyx R & D, Technology Development, Agrate Brianza (MB) – Italy*

18.10 ***Charge emission in SiO_2 layers containing Ge nanocrystals - evidence of a two-stage relaxation process from deep level transient spectroscopy analysis***

R. Beyer[1], H. Burghardt[1] and J. von Borany[2]

1 – Beyer Associates, Chemnitz, 2 – Institute of Ion Beam Physics and Materials Research, Forschungszentrum Dresden-Rossendorf,,Germany

18.30 **Poster session**

20.00 **Dinner**