Simplifying mixed-signal circuits in GaN

Selective plasma etching integrates E-mode and D-mode HEMTs for mixed-signal electronics

EUROPEAN researchers have developed a relatively simple approach for making a logic invertor with E-mode and D-mode GaN HEMTs.

Led by Jan Kuzmik from the Institute of Electrical Engineering, Slovak Academy of Sciences, the team produced its invertor by starting with the same epistructure for both types of devices, and then selectively etching the heavily doped *n*-type GaN cap layer in the gate trenches of the E-mode HEMT.

The researchers' effort is an important step in the development of GaN electronics for high-performance digital and analogue circuits. This field is very promising, thanks to advances in the design of E-mode HEMTs, and increases in transistor speed that stem from a self-aligned approach.

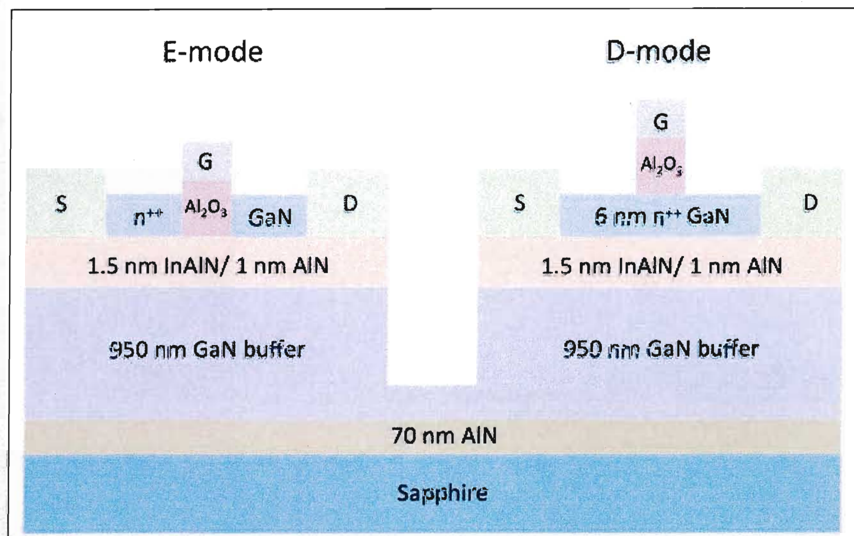
Creating fast mixed-signal circuits in GaN is not easy, however. Options employed by other groups are to turn to different epistructures for E-mode and D-mode devices, and to use a combination of a gate recess and an additional growth step for the Ohmic contacts.

Major merits of the approach of Kuzmik and co-workers are a single epistructure, and just one lithographic step for gate recessing, oxide deposition and metallisation.

What's more, their self-aligned approach eliminates the gate-space-charge extension towards the drain. This will allow faster devices by minimising the drain delay component.

Furthermore, unlike a two-step alignment process, no additional capacitance is introduced beyond the MOS gate footprint.

The challenge with the technology developed by Kuzmik and his colleagues is that the threshold voltage of the E-mode HEMT is governed by the gate recess. And determining the appropriate etching conditions is not as easy as it might first appear, because surface native oxides can inhibit the process.



Integrated E-mode and D-mode HEMTs

So, to determine the etching selectivity between the cap and barrier layer, it is essential to account for any differences between the etch rate of the bare (oxidised) barrier and the capped variant.

To determine the appropriate etching conditions, the researchers investigated the impact of the plasma etching process on different areas of the E-mode HEMT.

Recessing of the gate involved inductive-coupled plasma, reactive-ion etching with a mixture of $SiCl_4$ and SiF_6 for between 2 minutes and 5 minutes, using a pressure of 2.7 Pa. Measurements on the processed material revealed a GaN etch rate of 6 nm per minute – implying an optimal etch time for the gate recess of 150 s to 210 s – and indicated good selectivity with respect to InAlN.

Electrical measurements on a 2-inch wafer revealed an average E-mode HEMT threshold voltage of 0.8 V, and a value of -2.6 V for the D-mode variant. The spread in both devices across a 2-inch wafer was ±0.5 V.

Both classes of transitor exhibited a peak drain current of 0.35 A mm^{-1}. This similarity is encouraging, suggesting that etching did not compromise current.

Kuzmik's team also measured the transconductance of both devices.

The E-mode HEMT peaked at 110 mS/mm, while the D-mode variant was lower, but flatter. These differences are attributed to the larger channel-to-gate distance in the D-mode HEMTs, and the additional conduction in its heavily doped *n*-type GaN layer.

Measurements on the direct-coupled HEMT logic invertor using a 2.5 V supply voltage determined noise margins for the logic '0' and '1' levels of 137 mV and 812 mV, respectively.

The researchers claim that the invertor can be improved by tuning the technology and applying appropriate scaling to transistor dimensions.

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